REMARKS/ARGUMENTS

Applicants gratefully acknowledge the Examiner for notifying the Applicants of the reception of the IDS filed on 11/01/2004. Claims 18-21 have been cancelled.

Rejections under 35 U.S.C. 102(b)

In the Office Action mailed December 15, 2004, claims 1-23 are were rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 5,943,270 to Borkar (herein "*Borkar*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

As for claim 1, claim 1 as amended recites:

> A two-transistor DRAM cell comprising:
> a NMOS device with a gate;
> a PMOS device with a gate, the PMOS device coupled to the NMOS device; and
> a storage node coupled to at least one of the first and the second gates. [underline added]

In rejecting claim 1, the Examiner cites *Borkar* which disloses a two-transistor DRAM cell. In particular, the Examiner cites col. 4, lines 1-5 of Borkar which states " [w]hile FIG. **2** illustrates a dynamic memory cell **200** comprising two n-channel MOSFETs **205**, **210**, it should be apparent to those skilled in the art that p-channel MOSFETs (not shown) can also be employed in the present invention." The paragraph containing this sentence further goes on to state that "[t]o read data from a dynamic memory cell comprising two p-channel MOSFETS, the read bit line **215** would be precharged low, and then the read word line **225** would be asserted by making it high." As for these statements, Applicants are mystified as to how these statements anticipates claim 1 as alleged by the Examiner.

In particular, there is no disclosure or suggestion in the cited passage of coupling a PMOS and an NMOS device to form a two-transistor DRAM. At best, these statements suggests coupling two NMOS transistors or coupling two PMOS transistors

to form two different types of two-transistor DRAM cells and not combining one NMOS device with one PMOS device to form a single two-transistor DRAM cell. For at least these reasons, claim 1 is patentable over *Borkar*. Independent claims 4, 11 and 21 have similar features and therefore, are also patentable over *Borkar*.

Claims 2, 3, 5-10, 12-17, 22 and 23 depend from and add additional features to independent claims 1, 4, 11 and 21. Therefore, by virtue of their dependency, claims 2, 3, 5-10, 12-17,22 and 23 are also patentable over *Borker*.

Rejections under 35. U.S. C. 102(b)

In the Office Action claims 1-3, 21-23, are rejected under U.S.C. 102(b), as being anticipated by U.S. Patent No. 5,732,014 to Forbes (herein "*Forbes*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

As for claim 1, claim1 as amended recites:

> A two-transistor DRAM cell comprising:
> a NMOS device with a first gate;
> a PMOS device with a second gate, the PMOS device coupled to the NMOS device; and
> a storage node coupled to at least one of the first and the second gates. [underline added]
>]

The Examiner cites *Forbes* as anticipating claims 1-3 and 21-23 by citing FIG. 2, Col. 1, lines 11-14. However, FIG. 2 as well as the cited passage (i.e., col. 1, lines 11-14) does not disclose "a storage node coupled to at least one o the gates" as recited in amended claim 1. Instead, *Forbes* at best discloses coupling a storage node to a source electrode of an n-channel transistor. *See* col. 4, lines 22-32. For at least these treasons, claim 1 is patentable over *Forbes*. Claim 21 has also been amended to include similar features and is therefore, also patentable over *Forbes*.

Claims 2, 3, 22 and 23 depend from and add additional features to claims 1 and 21. Therefore, by virtue of their dependency to claims 1 and 21 claims 2, 3, 22 and 23 are also patentable over *Forbes*.

For at least the reasons provided above, Applicants respectfully request that these rejections of claims 1-17 and 21-23 be reconsidered and that claims 1-17 and 21-23 are in a condition for allowance.

CONCLUSION

In view of the foregoing, the Applicants respectfully submit that claims 1-17 and 21-23 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2009.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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